REMARKS

Claim Rejections – 35 U.S.C. §102(b) and §103(a)

The Examiner has rejected base Claim 1 and Claim 17 under 35 U.S.C. 102(b) and 103(a) as being anticipated by Kazunori et al and rendered obvious by additional references Ameritherm and Fujii et al. It is Applicant's understanding that Kazunori et al, Ameritherm, and Fujii et al fail to teach or render obvious the invention specified in claims 1-16 and claims 17-33.

Applicant claims in claims 1-33 a method of coupling a semiconductor die with a next level package. The method includes "providing at least one interconnect and arranging the semiconductor die, the next level package, and the at least one interconnect such that the at least one interconnect is disposed so as to be capable of joining the semiconductor die to the next level package." The method further comprises "generating an electromagnetic flux with an inductor, and *exposing the semiconductor die to the electromagnetic flux to induce eddy currents in the semiconductor die"* (claims 1-16) or *"exposing the at least one interconnect to the electromagnetic flux to induce eddy currents in the interconnect"* (claims 17-33) "to heat the semiconductor die and couple the semiconductor die with the next level package." That is, Applicant claims a method of coupling a semiconductor die with a next level package comprising inducing eddy currents in the semiconductor die or inducing eddy currents in at least one interconnect to heat the semiconductor die and couple the semiconductor die with a next level package as claimed in Claims 1-16 and 17-33 respectively.

It is Applicant's understanding that Kazunori et al fails to disclose a method of coupling a semiconductor die with a next level package comprising inducing eddy currents in a semiconductor die or interconnect as claimed by Applicant to heat the semiconductor die and couple the semiconductor die with a next level package. Kazunori et al does disclose a method of coupling a semiconductor die with a next level package but does not disclose inducing eddy currents in a semiconductor die or an interconnect. Instead, Kazunori et al discloses rolling a heating coil 2A around a heating block 1 to induce eddy currents for heating the heating block 1. Subsequently, heat transfers from

the heated heating block 1 to the solder bumps 6, which fuses the solder bumps 6 to electrically connect a semiconductor chip 5 (semiconductor die) and a circuit board 4 (next level package). Kazunori et al further discloses heating the semiconductor chip 5, solder bumps 6, or circuit board 4 through heat transfer from a heating block through convection to these components. Kazunori et al also discloses heating these respective components through heat transfer from the heating block through conduction to the circuit board and then to the other components. It is Applicant's understanding that heating the semiconductor chip 5, solder bumps 6, or circuit board 4 from heating block 1 through convection or conduction is not equivalent to a method of coupling a semiconductor die with a next level package comprising inducing eddy currents directly in the semiconductor die or interconnect.

Additionally, it is Applicant's understanding that neither of the secondary references, Ameritherm nor Fujii et al, discloses a method of coupling a semiconductor die with a next level package by inducing eddy currents in a semiconductor die or inducing eddy currents in at least one interconnect. Ameritherm discloses an induction heating system with the capability of generating a frequency of 13.56 MHz (+-5%) under 1 kW*/High Freq. However, Ameritherm fails to disclose a method of coupling a semiconductor die with a next level package by inducing eddy currents in a semiconductor die or inducing eddy currents in at least one interconnect. Fujii et al discloses a flexible substrate. However, Fujii et al also fails to disclose a method of coupling a semiconductor die with a next level package by inducing eddy currents in a semiconductor die or inducing eddy currents in at least one interconnect. As such, since Kazunori et al, Ameritherm, nor Fujii et al, teach a method of coupling a semiconductor die with a next level package by inducing eddy currents in a semiconductor die or inducing eddy currents in at least one interconnect the combination of references can not teach or render obvious Applicant's invention as claimed in Claims 1-33.